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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,184	02/27/2002	Alex N. Koltzoff	16159.025001;P6145	1434

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EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 03/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/085,184	KOLTZOFF ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☒ Claim(s) *6,15 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 18 are presented for examination.

Claim Objections

2. Claims 6, and 15 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claims 6, and 15, recite ' the integrated circuit comprises a texture engine '; however, the integrated circuit has not been positively recited as part of the invention claimed in claims 1 and 12, from which claims 6 and 15 depend.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 – 5, and 7 – 9, are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Watanabe et al. [hereinafter as Watanabe], US 5,926,837.

4. As to claim 1, Watanabe discloses an interface between memory [4, Memory] and an integrated circuit [5, memory controller, fig.2], comprising:

a. a write path [for writing the data signals from the data bus to the memory] comprising a write data path [Data bus] and a forwarded clock path [clock signal line]; and

b. a read path [for reading data from memory to data bus] comprising a read data path [Data bus], wherein data propagated through the write path and read path [data propagated through data bus] is synchronized by a clock signal [memory system operating in synchronization with the clock][col. 3, lines 15 – 18, col. 4, lines 37 – 60, fig. 2].

5. As to claim 2, Watanabe discloses write data path synchronized operations with the forwarded clock path, wherein the forwarded clock path and read path use the clock signal as a time reference [col. 5, 20 – 60, fig. 5].

6. As to claim 3, Watanabe discloses that the clock signal is provided by [clock generator of] the integrated circuit [5][fig. 2].

7. As to claim 4, Watanabe discloses that the read path and write path operatively connect the memory [4] and integrated circuit [5] [fig. 2].

8. As to claim 5, Watanabe discloses different types of the memory including a dynamic random access memory [DRAM], a static random access memory [SRAM], and a read only memory [ROM] therefore, he teaches SDRAM too [col. 5, lines 4 – 9].

9. As to claim 7, Watanabe discloses the write data path comprises circuitry [52, input buffer] having a first propagation time, wherein the forwarded clock path comprises circuitry [51, output buffer] having a second data propagation time, and wherein the first data propagation time is substantially equal to the second data propagation time [the output buffer and input buffer have the similar structure which inherently have substantially equal propagation time] [col. 4, lines 50 – 60, fig. 2].

10. As to claim 8, Watanabe discloses the read data path with pipeline circuitry adapted to reduce the timing skew between the clock signal and data which is output from each memory therefore, he teaches to compensate for accumulated phase generated by data propagation through the read data path too [col. 5, lines 14 – 67, fig. 5].

11. As to claim 9, Watanabe discloses the pipeline circuitry inputs at least one clock [CKn, n= 1 to 4] signal, and is dependent on the clock signal [CK0][col. 5, lines 13 – 23, fig. 2, 5].

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

13. Claims 1 – 5, 7 – 9, 10 – 14, and 16 – 17, are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Yoo et al. [hereinafter as Yoo], US Patent Application Publication 2002/0161968 A1.

14. As to claim 1, Yoo discloses an interface between memory [1, DRAM] and an integrated circuit [40, memory controller, fig.3], comprising:

a. a write path [for writing the data signals from the data bus to the memory] comprising a write data path [Data bus] and a forwarded clock path [WCLK, write clock]; and

b. a read path [for reading data from memory to data bus] comprising a read data path [Data bus], wherein data propagated through the write path and read path [data propagated through data bus] is synchronized by a clock signal [writing the data signals from data bus to the memory in synchronization with a first clock signal and reading data from the memory to the data bus in synchronization with the first clock and generates a second clock in response to the first clock, and the second clock is being used to receive data from bus by controller] [para 0007 - 0008 on page 1, para 0027 - 0030 on page 3, and para 0031 - 0032 on page 4].

15. As to claim 10, Yoo discloses a computer system having an interface dependent on a clock and having a write path [for writing the data signals from the data bus to the memory] and a read path [for reading data from memory to data bus] [para 0027 on page 3, fig. 3] comprising:

a. a memory [1, DRAM] , and

b. an integrated circuit [40, memory controller],

wherein the interface operatively connects the memory and integrated circuit, synchronizes write data propagating through the write path with a first clock signal [write clock] propagating through the write data path, and synchronizes read data propagating through the read path with a second clock signal [read clock] [para 0007 - 0008 on page 1, para 0027 -0030 on page 3, and para 0031 - 0032 on page 4].

16. As to claim 12, Yoo discloses a method for synchronizing data propagation through an interface connecting memory [44] and an integrated circuit, the interface having a write path and a read path, comprising:

a. propagating data through a write data path [for writing the data signals from the data bus to the memory], wherein the write path comprises the write data path and a forwarded clock path [write clock path];

b. propagating a clock signal [WCLK] through the forwarded clock path [write clock path];

c. synchronizing the data propagation through the write data path to the forwarded clock path [write clock path];

d. propagating data through a read data path [for reading data from memory, from 44 to 40], wherein the read path comprises the read data path; and

e. synchronizing the data propagation through the read data path to the clock signal [para 0007 - 0008 on page 1, para 0027 -0030 on page 3, and para 0031 - 0032 on page 4].

17. As to claim 2, Yoo discloses the write data path synchronizes operation with the forwarded clock path [WCLK], and wherein the forwarded clock path [WCLK] and read data path use the clock signal as a time reference [the phases of multiple second clock signals due to difference in propagation delay between each of the memory modules and the controller][para 0008 on page 1].

18. As to claims 3, and 13, Yoo discloses that a clock signal is received from the integrated circuit [40][controller is generating a first clock signal][para 0007 on page 1, fig. 3].

19. As to claims 4, and 16, Yoo discloses that the read path and write path operatively connect the memory [DRAM] and integrated circuit [40] [fig. 3].

20. As to claims 5, and 14, Yoo discloses different types of memory including the SDRAM memory [para 0003 on page 1].

21. As to claim 7, Yoo discloses that a first amount of propagation delay needed through wrote path is substantially equal amount to the second amount of propagation delay through the forwarded clock [para 0008 on page 1].

22. As to claim 17, Yoo discloses that a first amount of propagation delay needed through wrote path is substantially equal amount to the second amount of propagation delay through the forwarded clock [para 0008 on page 1].

23. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested to the applicant in preparing responses, to fully consider the references in entirely as potentially teaching all or part of claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

24. **Prior Art not relied upon:** Please refer to the references listed in attached PTO-892, which, are not relied upon for rejection since these references are relevant to the claimed invention.

Allowable Subject Matter

25. Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 6:45 am to 5:15 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
March 1, 2005

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
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